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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/550,642	04/14/2000	David F. Sorrells	1744.0920001	9236

7590 11/18/2004

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EXAMINER
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ODOM, CURTIS B

ART UNIT	PAPER NUMBER
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2634

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/550,642

Applicant(s)

SORRELLS ET AL.

Examiner

Curtis B. Odom

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on 03 August 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 75-81,83-92,94-104,106-115 and 117-119 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 75,76,79-81,83-87,90-92,94-100,103,104,106-110,113-115 and 117-119 is/are rejected.
- 7) ☒ Claim(s) 77,78,88,89,101,102,111 and 112 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 April 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- 1) ☐ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948)     | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date. _____  | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### ***Response to Arguments***

1. The term “couple” is defined as “something that joins or links two things together” (see “Merriam-Webster’s Collegiate Dictionary”, Tenth Edition, page 265). Therefore, it is the understanding of the examiner that two components are “coupled” to each other as long as there is a link between the two components. The components may also be coupled (linked) to each other through other components. Thus, it is the understanding of the examiner that components may be coupled to each other without being directly connected to one another.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 75, 79, 81, 83, 86, 90, 92, 94, 97, 98, 106, 109, 113, and 115, and 117 are rejected under 35 U.S.C. 102(e) as being anticipated by Bonn et al. (previously cited in Office Action 6/7/2004).

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Regarding claim 75, Bonn et al. discloses an apparatus (Fig. 1, block 10, column 2, line 8-column 4, line 30) for down-converting an electromagnetic signal, wherein an RF signal is an electromagnetic signal, comprising:

- a capacitor (Fig. 1, element 56) having a first and second port;
- a transistor (Fig. 1, elements 20, 50, and 30) having a source, gate, and drain; and
- a resonant structure having a first and second port (Fig. 1, elements 38 and 42, capacitor and inductor);

wherein the first port of the capacitor (Fig. 1, element 56) is electrically coupled one of the source or drain of the transistor (elements 50), and the first port of the resonant structure (input to element 38) is electrically coupled to the other of the source or drain of the transistor (Fig. 1, element 50), wherein the resonant structure is electrically coupled to the source and drain of the transistor through the gate of the transistor ; and

wherein a control signal (Fig. 1, LO) is electrically coupled to the gate of the transistor (Fig. 1, element 50), and an RF source signal (Fig. 1, RF) is electrically coupled to the gate of the first port of the resonant structure (Fig. 1, elements 38 and 42), and

wherein a signal frequency at the first port of the capacitor (Fig. 1, element 65, IF) is lower than a frequency of the RF source signal.

Regarding claim 79, which inherits the limitations of claim 75, Bonn et al. discloses the first port of the capacitor (Fig. 1, element 65) is electrically coupled to an impedance matching network (Fig. 1, block 11, column 2, lines 8-27).

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Regarding claim 81, which inherits the limitations of claim 75, Bonn et al. discloses the first port of the resonant structure (Fig. 1, elements 38 and 42) is coupled to an impedance matching network (Fig. 1, block 11, column 2, lines 8-27).

Regarding claim 83, which inherit the limitations of claim 75, Bonn et al. discloses the transistor is a FET (column 2, line 66-column 3, line 12).

Regarding claim 86, Bonn et al. discloses an apparatus (Fig. 1, block 10, column 2, line 8-column 4, line 30) for down-converting an electromagnetic signal, wherein an RF signal is an electromagnetic signal, comprising:

- a first and second (Fig. 1, elements 26, 44, and 56) capacitor each having a first and second port;

- a transistor (Fig. 1, elements 20, 50, and 30) having a source, gate, and drain; and

- a resonant structure having a first and second port (Fig. 1, elements 38 and 42, capacitor and inductor);

wherein the first port of the first capacitor (Fig. 1, element 56) and the second port of the second capacitor (Fig. 1, element 44) are electrically coupled to one of the source or drain of the transistor (element 50, wherein the second port of the second capacitor is electrically coupled to the source and drain of the transistor through the gate of the transistor), the first port of the second capacitor (Fig. 1, element 44) and the first port of the resonant structure (Fig. 1, elements 38 and 42) are electrically coupled to the other of the source and the drain of the transistor; and

wherein a control signal (Fig. 1, LO) is electrically coupled to gate of the transistor, and an RF source signal (Fig. 1, RF) is electrically coupled to the first port of the resonant structure, and

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wherein a signal frequency (IF) at the first port of the first capacitor (Fig. 1, element 56) is lower than a frequency of the RF source signal.

Regarding claims 90, 92, and 94, which inherit the limitations of claim 86, the claimed device includes features corresponding to subject matter mentioned above in the rejection of claims 79, 81, and 83 which is applicable hereto.

Regarding claim 97, Bonn et al. discloses an apparatus (Fig. 1, block 10, column 2, line 8-column 4, line 30) for down-converting an electromagnetic signal, wherein an RF signal is an electromagnetic signal, comprising:

- a capacitor (Fig. 1, element 65) having a first and second port;

- a first and second transistor (Fig. 1, elements 20, 30 and 50) each having a gate, drain, and source; and

- wherein the first port of the capacitor (element 65) is electrically coupled to one of the drain or source of the first transistor (element 50), and the second port of the capacitor is electrically coupled to the one of the drain or source of the second transistor (element 30, wherein the capacitor is coupled to the second transistor through the first transistor), and the gate of the first transistor is electrically coupled to the gate of the second transistor (Fig. 1, elements 30 and 50); and

- wherein a control signal (Fig. 1, LO and Mixer Enable) is electrically coupled to the gate of the first transistor and the gate of the second transistor, and an RF source signal (Fig. 1, RF) is electrically coupled to the other of the drain or source of the first transistor (Fig. 1, element 50) and the other of the drain or source of the second transistor (Fig. 1, element 30), and

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wherein a signal frequency (RF) at the first port of the capacitor (Fig. 1, element 56) is lower than a frequency (IF) of the RF source signal.

Regarding claim 98, which inherits the limitations of claim 97, Bonn et al. discloses a resonant structure having a first and second port (Fig. 1, elements 38 and 42),

wherein the first port of the resonant structure is electrically coupled to the other of the drain or source of the first transistor (Fig. 1, element 50) and second port of the resonant structure is coupled to the other of the drain or source of the second transistor (Fig. 1, element 30).

Regarding claims 106, which inherit the limitations of claim 97, Bonn et al. discloses the transistors are FETs (column 2, line 66-column 3, line 12).

Regarding claim 109, Bonn et al. discloses an apparatus (Fig. 4 and 5, column 6, lines 3-67) for down-converting an electromagnetic signal, wherein an RF signal is an electromagnetic signal, comprising:

a first and second (Fig. 1, elements 26, 44, and 56) capacitor each having a first and second port;

a transistor (Fig. 1, elements 20, 50, and 30) having a source, gate, and drain; and

a load (Fig. 4, elements 58, 32, 46, and 48);

wherein the first port of the first capacitor (Fig. 1, element 56) and the first port of the second capacitor (Fig. 1, element 44) are electrically coupled to one of the source or drain of the transistor (element 50, wherein the first port of the second capacitor is electrically coupled to the source and drain of the transistor through the gate of the transistor), the load (Fig. 1, element 46)

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and the second port of the second capacitor (Fig. 1, element 44) are electrically coupled to the other of the source and the drain of the transistor; and

wherein a control signal (Fig. 1, LO) is electrically coupled to gate of the transistor, and an RF source signal (Fig. 1, RF) is electrically coupled to the first port of the transistor, and

wherein a signal frequency (IF) at the first port of the first capacitor (Fig. 1, element 56) is lower than a frequency of the RF source signal.

Regarding claim 113, which inherits the limitations of claim 109, Bonn et al. discloses the first port of the capacitor (Fig. 1, elements 26) is electrically coupled to an impedance matching network (Fig. 1, block 11, column 2, lines 8-27).

Regarding claim 115, which inherits the limitations of claim 109, Bonn et al. discloses the first port of the second capacitor (Fig. 1, element 44) is coupled to an impedance matching network (Fig. 1, block 11, column 2, lines 8-27).

Regarding claims 117, which inherit the limitations of claim 109, Bonn et al. discloses the transistor is a FET (column 2, line 66-column 3, line 12).

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.



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5. Claims 76, 80, 84, 85, 87, 91, 95, 96, 99, 100, 103, 104, 107, 108, 110, 114, 118, and 119 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bonn et al. (previously cited in Office Action 6/7/2004).

Regarding claims 76, 87, 100, 110, Bonn et al. does not disclose a value of capacitance for the capacitor is selected so that the capacitor discharges stored energy to a load when the transistor is open. However, Bonn et al. discloses a capacitor coupled to a transistor (Fig. 1, element 20) connected in series with a load (Fig. 1, block 32). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that in order for the device to function properly the value of the capacitor would need to be correctly calculated for the capacitor to function properly. Thus, choosing a value for the capacitor is deemed a design choice and does not constitute patentability.

Regarding claims 80, 91, 103, 104 and 114, Bonn et al. does not disclose the first port of the capacitor is electrically coupled to an amplifier or the first and second ports of the capacitor is electrically coupled to the first and second ports of a differential amplifier. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of an amplifier to amplify weaker signals which would allow more efficient processing.

Regarding claims 84, 85, 95, 96, 107, 108, 118, and 119, Bonn et al. does not disclose the transistor is a JFET or MOSFET. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that since these are all transistors, that each of these devices could have been used to perform the switching function. Thus, choosing a type of transistor is deemed a design choice and does not constitute patentability.

Regarding claim 99, Bonn et al. discloses a first impedance each having a first and second port (Fig. 1, block 11, column 2, lines 8-27),

wherein the first port of the first impedance is electrically coupled to the first port of a resonant structure (Fig. 1, elements 38 and 42) wherein an RF source signal (Rf) is electrically coupled to the second port of the first impedance.

Bonn et al. does not disclose a second impedance having a first and second port wherein the first port of the second impedance is electrically coupled to the second port of a resonant structure, and wherein an RF source signal (Rfin) is electrically coupled to the the second port of the second impedance. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a second impedance which could perform the same function as the first impedance to provide a desired impedance for processing of the signal at a certain structure within the device. Thus, claim 99 does not constitute patentability.

#### ***Allowable Subject Matter***

6. Claims 77, 78, 88, 89, 101, 102, 111, and 112 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### ***Conclusion***

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 571-272-3046. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Curtis Odom



**STEPHEN CHIN**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER**

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November 1, 2004